REMARKS

Claims 1-5 were pending. All were rejected. The Applicant has amended claims 1-4 and added new claims 6-24. Therefore, claims 1-24 are presently pending. The Applicants requests further consideration and re-examination in view of the amendments above and remarks set forth below.

Objection to the Abstract

The Abstract was objected to for not reflecting an inventive feature to distinguish over the prior art. The Applicant has amended the Abstract to include an additional feature of claim 1. As explained below, claim 1 distinguishes over the prior art at least because of this feature. Thus, the Abstract now reflects an inventive feature.

The Examiner stated that amendments to the abstract need to be on separate sheet without brackets and underlines in addition to a mark-up copy. The Applicant is unable to confirm the existence of this stated requirement that the abstract needs to be provided without brackets and underlines in the current rules governing amendment practice. Rather, *Office Flyer: Amendments May Now be Submitted in Revised Format*, (posted 30 June 2003), states that 37 CFR 1.121 has been revised to no longer require two versions (a clean version and a marked up version) of each replacement paragraph or section, or amended claim. Accordingly, the Applicant has submitted the amendments to the Abstract with brackets and underlining in accordance with the *Changes to Implement Electronic Maintenance of Official Patent Application Records, Final Rule*, published at 68 Fed. Reg. 38611 (30 June 2003).

Rejections under 35 U.S.C. § 112

Claims 1-5 were rejected as being indefinite for various reasons. The Applicant has amended claims 1-4 so as to overcome these rejections. Particularly, claim 1 has been amended to no longer refer to "said other function units"; claim 2 has been amended to recite that the mapping is used to determine the new value of the pointers; claim 3 has been amended to clarify the relationship of the super instructions to the limitations of the base claim; and claim 4 is amended to no longer recite "said super instruction." Claim 4 now recites that at least one of the instruction sequences

comprises at least one no op instruction. Support for this feature can be found in the Applicant's specification at least at page 2, lines 26-30 and page 7, lines 1-2.

In view of the above, the Applicant submits that claims 1-5 are not indefinite.

Rejections under 35 U.S.C. § 102

Claims 1 and 5 were rejected as being unpatentable in view of Sowa, EP 284,364. Sowa was not applied to claims 2-4.

The Applicant disagrees that Sowa discloses the claimed feature that the local memories comprise instructions of different length. In fact, Sowa does not discuss instruction length at all. Regarding Sowa, the Examiner stated that the instructions of Sowa "can be any length, there is no length restriction." The Applicant respectfully submits that the Examiner is not applying the correct legal standard for anticipation or inherency under 35 U.S.C. §§ 102. As is stated in Section 2112 of the Manual of Patent Examining Procedure (MPEP), "[t]he fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic." (Emphasis in original), citing *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); and *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). In this same section, the MPEP further states that "[t]o establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" (Emphasis added), quoting *In re Robertson*, 169 F.2d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). Thus, Sowa does not suggest or disclose that instructions of different lengths. For at least this reason, claim 1 is allowable over Sowa. Claim 5 is allowable at least because it is dependent from claim 1.

Further, as explained in the Applicant's specification at page 6, lines 30-34, each machine cycle is represented by one row of operations in a table, while columns in the table correspond to the functional units upon which the operations are executed. All of the operations in a given row are issued simultaneously on the corresponding machine cycle, one per function unit. The Applicant has amended claim 1 so that claim 1 now recites that each function unit executes instructions according to machine

cycles, each function unit executing one instruction per machine cycle. Sowa does not suggest or disclose such a feature. This is clear because Sowa at col. 5, lines 1-11, states that synchronization among processors is achieved by halting operation on one processor while waiting for an operation to complete on another processor. Further, Sowa was not applied to original claim 4, which substantially included this feature. Because Sowa does not suggest or disclose such a feature, this is another reason why claim 1 is allowable over Sowa. Since claim 5 is dependent from an allowable base claim 1, this is also another reason why claim 5 is allowable.

New claims

New claim 6 recites at least one processing section that remains idle for the duration of a super instruction. Support for this feature can be found in the Applicant's specification at least at page 7, lines 18-21. New claim 6 is allowable at least because it is dependent from an allowable base claim 1.

New claim 7 recites that a super instruction comprises a tuple for each processing section that is not idle for the duration of the super instruction and wherein each tuple identifies a function unit on which execution occurs and a number of memory words needed to represent corresponding operations to be executed on the function unit. Support for this feature can be found in the Applicant's specification at least at page 7, lines 4-21. New claim 7 is allowable at least because it is dependent from an allowable base claim 1.

New claim 8 recites that a super instruction indicates a total number of machine cycles for the super instruction. Support for this feature can be found in the Applicant's specification at least at page 7, lines 7-8. New claim 8 is allowable at least because it is dependent from an allowable base claim 1.

New claim 9 recites that the local memories are loaded at a start of the program. Support for this feature can be found in the Applicant's specification at least at page 8, lines 10-11. New claim 9 is allowable at least because it is dependent from an allowable base claim 1.

New claim 10 recites that the local memories are loaded at the time of a branch to a super instruction. Support for this feature can be found in the Applicant's specification at least at page 8, lines 11-12. New claim 10 is allowable at least because it is dependent from an allowable base claim 1.

New claim 11 recites a fall-through super instruction is executed when a super instruction executes without branching. Support for this feature can be found in the Applicant's specification at least at page 8, lines 24-31 and at page 10, line 30 to page 11, line 7. New claim 11 is allowable at least because it is dependent from an allowable base claim 1.

New claim 12 recites that the function unit of each processing section executes instructions stored in the local memory "according to machine cycles, each function unit executing one instruction per machine cycle." As discussed above, Sowa does not suggest or disclose such a feature. New claim 12 is allowable for at least this reason.

New claim 13 recites that the linear block of code of the super instruction can only be entered at a starting address and includes one or more branch instructions, similarly to original claim 1. New claim 13 is allowable at least because it is dependent from an allowable base claim 12.

New claim 14 recites that the pointers in each of the processing sections are reset to a new value determined by a target address of one of the branch instructions when a function unit branches in response to that branch instruction, similarly to original claim 1. New claim 14 is allowable at least because it is dependent from an allowable base claim 12.

New claim 15 recites that the target address of at least one of the branch instructions corresponds to a starting address of a super instruction in the program, similarly to original claim 3. New claim 15 is allowable at least because it is dependent from an allowable base claim 12.

New claim 16 recites a memory for determining the new value of the pointers, the memory storing a mapping for each target address specifying one of the pointer values for each of the pointers corresponding to that target address, similarly to original claim 2. New claim 16 is allowable at least because it is dependent from an allowable base claim 12.

New claim 17 recites that at least one of the instruction sequences comprises at least one no op instruction. Support for this feature can be found in the Applicant's specification at least at page 2, lines 26-30 and page 7, lines 1-2. New claim 17 is allowable at least because it is dependent from an allowable base claim 12.

New claim 18 recites that the instruction sequences comprise instructions of different lengths, similarly to original claim 1. New claim 18 is allowable at least because it is dependent from an allowable base claim 12.

New claim 19 recites at least one processing section that remains idle for the duration of the super instruction. Support for this feature can be found in the Applicant's specification at least at page 7, lines 18-21. New claim 19 is allowable at least because it is dependent from an allowable base claim 12.

New claim 20 recites that the super instruction comprises a tuple for each processing section that is not idle for the duration of the super instruction and wherein each tuple identifies a function unit on which execution occurs and a number of memory words needed to represent corresponding operations to be executed on the function unit. Support for this feature can be found in the Applicant's specification at least at page 7, lines 4-21. New claim 20 is allowable at least because it is dependent from an allowable base claim 12.

New claim 21 recites that the super instruction indicates a total number of machine cycles for the super instruction. Support for this feature can be found in the Applicant's specification at least at page 7, lines 7-8. New claim 21 is allowable at least because it is dependent from an allowable base claim 12.

New claim 22 recites that the local memories are loaded at a start of a program that includes the super instruction. Support for this feature can be found in the Applicant's specification at least at page 8, lines 10-11. New claim 22 is allowable at least because it is dependent from an allowable base claim 12.

New claim 23 recites that the local memories are loaded at the time of a branch to the super instruction. Support for this feature can be found in the Applicant's specification at least at page 8, lines 11-12. New claim 23 is allowable at least because it is dependent from an allowable base claim 12.

New claim 24 recites a fall-through super instruction is executed when the super instruction executes without branching. Support for this feature can be found in the Applicant's specification at least at page 8, lines 24-31 and at page 10, line 30 to page 11, line 7. New claim 24 is allowable at least because it is dependent from an allowable base claim 12.

Conclusion

In view of the above, the Applicant submits that all of the pending claims are now allowable. Allowance at an early date would be greatly appreciated. Should any outstanding issues remain, the examiner is encouraged to contact the undersigned at (408) 293-9000 so that any such issues can be expeditiously resolved.

Respectfully Submitted,

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Derek J. Westberg (Reg. No. 40,872)